CLAIMS:

1. A programmable controller including:

at least one user input interface and an input register for connection to process plant and/or machinery to provide sampled and stored input data in digital form,

at least one user output interface and an output register for connection to process plant and/or machinery to receive and store output data in digital form,

programmable logic hardware including a plurality of basic logic elements and electrically configurable interconnections, said interconnections configurable to interconnect the logic elements as a user control program circuit and to connect the user control program circuit to said input and output interfaces,

program loading means to enable the user to configure the programmable logic hardware as a circuit implementing a user control program prior to initiating control of the associated process plant and/or machinery.

2. A programmable logic controller as claimed in claim 1 including a user control program implemented as an electrical logic circuit in said programmable logic hardware, with said user program circuit connected to said input and output interfaces.

3. A programmable controller as claimed in claim 2, for use with a monitoring device, and wherein:

said programmable logic as configured has a plurality of state data storage units storing the user program circuit state data, and a means of access to said state data storage units,

said monitoring device may be connected via said means of access to said state data storage units, and

said means of access to said state data storage units enables said monitoring device to read data values from said state data storage units and to write data values to said state data storage units while the user control program continues to perform control functions.

4. A programmable controller as claimed in claim 3 with an operating cycle of at least two non-overlapping sequential intervals, and wherein,

said input data register operates to sample and store the input data within a first said interval ("logic processing interval"),

said programmable logic circuit includes clocking means that applies clock pulses in said logic processing interval as required by the user control program circuit, said logic processing interval allowing the user control program circuit signals to settle, and

said means of access to said data storage units enable said monitoring device to read data from and/or write to said state data storage units during a second said interval ("data access interval").

5. A programmable controller as claimed in claim 4 including means to support state data modification comprising:

secondary modification data storage corresponding to said state data storage units, and

a modification indicator corresponding to each said state data storage unit, said modification indicator and the contents of said secondary storage being writable by said monitoring device; and

data modification means operative to perform within one said data access interval the steps of:

scanning said modification indicators,

loading data stored in said secondary modification data storage units to said corresponding state data storage units if the corresponding modification indicator so indicates, and

resetting said modification indicators.

6. A programmable controller as claimed in claim 4 including means to support state data forcing comprising:

secondary modification data storage corresponding with said state data storage units

a data forcing indicator for each said storage unit, said data forcing indicator and the contents of said secondary storage being writable by said monitoring device; and

data modification means operative to perform within one said data access interval the steps of:

scanning said data forcing indicators,

loading data stored in said secondary storage units to said corresponding state data storage units if the corresponding data forcing indicator so indicates,

without resetting said data forcing indicators.

7. A programmable controller as claimed in claim 4 including means to support program swap operations, adapted to perform, during said data access interval, the steps of:

reading and storing state data from said state data storage units,

configuring a new user control program in said programmable logic by reconfiguring said programmable connections; and

writing said stored state data, or modified stored state data, to corresponding newly configured state data storage units.

8. A programmable controller as claimed in claim 4 with duplicated hardware to facilitate program swapping operations including:

at least two separately configurable sections of programmable logic hardware for separately configurable user control program circuits,

output selector means to selectively connect one of said programmable logic hardware sections to said output interfaces via the output register, and

means to support program swap operations adapted to perform the steps of:

configuring a new user control program in incoming said programmable logic hardware section not connected to said output interface, and

subsequently, all within one said data access interval:

reading state data from said storage units of the outgoing said programmable logic hardware section,

optionally writing the state data from the outgoing said programmable logic hardware section into the incoming said programmable logic hardware section so that the data is written to the state data storage units that have the same user control program functions as those from which it was read,

disconnecting said outgoing programmable logic hardware section from said output interfaces, and

connecting said incoming programmable logic device to said output interface via the output register.

9. A programmable controller as claimed in claim 4 including means to support relocation of state data from the outgoing programmable logic hardware section to the corresponding state data storage unit in the incoming programmable logic hardware section including:

relocation address storage corresponding with said state data storage units

secondary state data storage to save data from said state data storage units

selection means to select either a non-relocated address or a relocated address with which to access the said secondary state data storage, and

data relocation means performing the steps of:

(i) loading said secondary relocation address storage with addresses supplied by said monitoring device; and within one said data access interval,

(ii) reading a state data bit from a programmable logic hardware section,

(iii) writing said state data bit into said secondary state data storage at an address stored in said relocation address storage,

(iv) repeating steps (ii) and (iii) until all required bits have been relocated and transferred,

(v) reading a state data bit from said secondary state data storage,

(vi) writing said state data bit into the same or a different programmable logic hardware section at the same address at which it was located in said secondary state data storage, and

(vii) repeating steps (v) and (vi) until all required bits have been transferred

10. A programmable controller as claimed in claim 2 including means to support circuit failure detection including

at least two separately configurable sections of programmable logic hardware configurable with identical user control program circuits and with identical input values, and,

failure detection means comparing a set of output values of each said programmable logic section with the corresponding set of output values of each other section, and indicating failure of said programmable logic hardware if the sets of settled output values of said sections are not identical.

11. A programmable controller as claimed in claim 2 including means to support circuit failure detection and correction including:

at least three said separately configurable sections of programmable logic hardware configurable with identical user control program circuits and with identical input values, and

failure detection means to compare a set of output values of each said programmable logic hardware section with the corresponding set of output values of at least two other said sections, and

output processing means to pass a set of correct output values to the control outputs via the output register and ensure incorrect output values as indicated by said failure detection means do not propagate to the control outputs;

wherein said failure detection means determines that a programmable logic hardware section has failed if the set of settled output values of said programmable logic hardware section is not identical to at least one of the sets of settled output values of the other programmable logic hardware sections, identifies any unmatched sets of outputs as coming from a failed programmable logic hardware section, and indicates the failure of that programmable logic hardware section.

12. A programmable controller as claimed in claim 10 including a plurality of said failure detection means with the sets of outputs from each section of programmable logic hardware provided as inputs to each said failure detection means, and

detection of a failure by any one of the two or more failure detection means indicates that a failure has occurred.

13. A programmable controller as claimed in claim 11 including a plurality of said failure detection and correction means with the sets of outputs from each of the at least three sections of programmable logic hardware provided as inputs to each of the failure detection and correction means, and wherein:

indication of a difference between the sets of output values of any two sections of programmable logic hardware by any one or more of the failure detection means indicates that a failure has occurred, and

at least two or more failure detection circuits must agree that a particular section of programmable logic hardware is operating correctly before the set of output values from that said section is deemed to be correct, and

said output processing means passes a set of correct output values to the control outputs via the output register and ensures incorrect output values, as indicated by said failure detection means, are not propagated to the control outputs.

14. A programmable controller as claimed in claim 13 including exception evaluating and handling means which ensures that the controller responds appropriately when the number of sets of concurrently correct output values deemed desirable as a safety margin does not exist, the

minimum said number being two.

15. A programmable controller as claimed in claim 2 wherein said programmable controller receives input signals from duplicate sensors and said user control program includes at least one input signal monitoring function block, said monitoring block determining the invalidity of an input signal by a comparison of said duplicate input signals using criteria defined as part of the function block as suitable to identify signals in error, and indicating an input signal error if said input signal is deemed invalid.

16. A programmable controller as claimed in claim 15 wherein said duplicate sensors include three or more matching sensors and the respective said input signal monitoring function block determines the invalidity of an input signal from a comparison of said matching input signals, and determines the invalid signal as the odd-one-out, and passes a single copy of the valid signals as the input signal.

17. A programmable controller as claimed in claim 4 including means to support circuit failure detection including

at least two separately configurable sections of programmable logic hardware configurable with identical user control program circuits and with identical input values, and,

failure detection means comparing a set of output values of each said programmable logic section with the corresponding set of output values of each other section, and indicating failure of said programmable logic hardware if the sets of settled output values of said sections are not identical.

18. A programmable controller as claimed in claim 4 including means to support circuit failure detection and correction including:

at least three said separately configurable sections of programmable logic hardware configurable with identical user control program circuits and with identical input values, and

failure detection means to compare a set of output values of each said programmable logic hardware section with the corresponding set of output values of at least two other said sections, and

output processing means to pass a set of correct output values to the control outputs via the output register and ensure incorrect output values as indicated by said failure detection means

do not propagate to the control outputs;

wherein said failure detection means determines that a programmable logic hardware section has failed if the set of settled output values of said programmable logic hardware section is not identical to at least one of the sets of settled output values of the other programmable logic hardware sections, identifies any unmatched sets of outputs as coming from a failed programmable logic hardware section, and indicates the failure of that programmable logic hardware section.

19. A programmable controller as claimed in claim 18 including a plurality of said failure detection and correction means with the sets of outputs from each of the at least three sections of programmable logic hardware are provided as inputs to each of the failure detection and correction means, and wherein:

indication of a difference between the sets of output values of any two sections of programmable logic hardware by any one or more of the failure detection means indicates that a failure has occurred, and

at least two or more failure detection circuits must agree that a particular section of programmable logic hardware is operating correctly before the set of output values from that said section is deemed to be correct, and

said output processing means passes a set of correct output values to the control outputs via the output register and ensures incorrect output values, as indicated by said failure detection means, are not propagated to the control outputs.

20. A programmable controller as claimed in claim 4 wherein said programmable controller receives input signals from duplicate sensors and said user control program includes at least one input signal monitoring function block, said monitoring block determining the invalidity of an input signal by a comparison of said duplicate input signals using criteria defined as part of the function block as suitable to identify signals in error, and indicating an input signal error if said input signal is deemed invalid.

as illustrated by the accompanying drawings.